UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,874	10/21/2003	Anatoliy V. Tsyrganovich	ZIL-521-1P	6810

47713 7590 08/23/2005

SILICON EDGE LAW GROUP LLP
6601 KOLL CENTER PARKWAY, SUITE 245
PLEASANTON, CA 94566

EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/690,874	TSYRGANOVICH, ANATOLIY V.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7,12 and 13* is/are allowed.

6)☒ Claim(s) *1-3,8-11,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 6/13/2005 has been reviewed and considered with the following results:

As to the objection to the specification, Applicant's amendment has overcome the objection, as such; the objection has been withdrawn.

As to the prior art rejections to claims 4-7, 12 and 13, Applicant's amendment has overcome the prior art rejections, as such; the prior art rejections have been withdrawn.

As to the prior art rejections to claims 1-3, 8-11, 14, and 15, Applicant's arguments with respect to the prior art rejections by the previous office action mailed on 5/06/2005 have been fully considered but are not deemed to be persuasive. Therefore, the prior art rejection is maintained. The arguments supporting the previous rejections are addressed in detail below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Mergard et al. (US 6,401,156; previously cited).

With regard to claims 1 and 2, Mergard et al. discloses in Figs. 2&10 a microcontroller integrated circuit, comprising a terminal; a crystal oscillator circuit (124) coupled to the terminal, the crystal oscillator circuit (a crystal oscillator generates a signal having a frequency of 32,768 Hertz in a manner well known in the art as shown in Fig. 4 of Hoague US Patent No. 6,186,140) outputting a first clock signal of a first frequency (32,768 Hz.); a real time clock (116) that receives the first clock signal; a processor (100) having a clock input lead; and an inherent clock multiplier circuit. One of ordinary skill in the art would understand that the circuit of Mergard et al. inherently comprises a clock multiplier circuit, which uses a low frequency clock signal of the oscillator circuit for multiplying that frequency for providing a high frequency clock signal for other circuits such as the processor (see below discussed with regard to claim 16).

With regard to claim 11, the reference also meets the recited limitations in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. in view of Ferraiolo et al. (US 5,757,238; previously cited).

With regard to claims 3 and 8-10, the above discussed circuit of Mergard et al. meets all of the claimed limitations except that Mergard et al. does not discloses details of the clock multiplier circuit such as the clock multiplier circuit includes a frequency locked loop, the frequency locked loop including a digital filter. Ferraiolo et al. teaches in Fig. 2 a clock multiplier circuit (200) comprising a frequency locked loop (200), the frequency locked loop including a digital filter (214, 216) for reducing the need and time required for the phase comparator operation to drive the PLL to lock. Therefore, it would have been obvious to one of ordinary skill in the art to implement the clock multiplier circuit taught by Ferraiolo et al. with the prior art (Fig. 2 of Mergard et al.) in order to quickly achieve phase lock at the different operating frequency for the circuit. The multiple is an integer (M) that can be changed by the processor (202, 204 in addition to 100 in Figs. 2&10 of Mergard et al).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al.

The above discussed circuit of Mergard et al. meets all of the claimed limitations except for the intended use the microcontroller in a battery-powered device, as the claimed structure is met by the prior art, the intended use of the circuit is likewise met. Recall that it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987.). The first frequency (32,768 Hz.) is less than 5 megahertz. Furthermore, Mergard et al. discloses all the claimed subject matter except for specifying that the second frequency is greater than 100 megahertz. It

would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to set a certain frequency range to meet the specific condition of the particular application. It has been held that discovering an optimum range or to optimally match to an application is obvious to the skilled artisan. See *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. in view of Gulliver et al. (US 6,150,889; previously cited).

The above discussed circuit of Mergard et al. meets all of the claimed limitations except for additional clock as a third clock signal (603 in instant Fig. 9) on the second terminal can be supplied to the clock input lead of the clock multiplier circuit rather than the first clock signal (615). Gulliver et al. teaches in Fig. 3 a circuit including an additional clock similar to the third clock recited in the claim. Therefore, it would have been obvious to one of ordinary skill in the art to implement the additional clock as a third clock signal taught by Gulliver et al. with the prior art (Fig. 2 of Mergard et al.) in order to provide a backup clock signal in the event of a failure of the first clock signal, and selection of the clock signals can be changed by the processor as well.

8. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergard et al. in view of Adams (US 5,638,010).

With regard to claim 16, Mergard et al. discloses in Figs. 2&10 a device comprising a processor (100) and a low frequency external crystal (124) exhibiting a first frequency (32768 Hz). The reference circuit meets all the claimed limitations except for a frequency locked loop (609 in instant Fig. 8), wherein the frequency locked loop receives a first clock signal having the

first frequency and generates therefrom a second clock signal, the second clock signal having a second frequency that is a multiple of the first frequency, wherein the second clock signal is supplied to the clock input lead of the processor. As disclosed in the US Patent 6,401,156; oscillators in the device of Mergard et al. are the low frequency clocks, but the processor (see column 7, line 60 through column 8, line 2) is operated at very high frequency clocks, which can be up to 200 MHz clock (see US Pat. 6,282,589). Therefore, one of ordinary skill in the art would infer that the device of Mergard et al. inherently comprises at least a clock multiplier circuit that receives the low frequency clocks from the oscillators and then generates the high frequency clocks to the processor (see Figs. 1-4 of Wilber; US Pat. 6,862,605; previously cited); and there are vast varieties of clock multiplier circuits which are well known in the art including the frequency locked loop. Adams teaches in Figs. 3-6 a circuit having a frequency locked loop as a clock multiplier circuit, wherein the frequency locked loop receives a first clock signal having the first frequency and generates therefrom a second clock signal, the second clock signal having a second frequency that is a multiple of the first frequency. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that frequency locked loop circuit taught by Adams in the device of Mergard et al. in order to meet the specific condition of the particular application.

With regard to claim 17, the frequency locked loop includes a ramp generator (68 and 70 in Fig. 3 of Adams).

Claims 18 and 20 are rejected for similar motivations; note the above discussion with regard to claims 16 and 17.

With regard to claim 19, the means (aka frequency locked loop) comprises a digital filter (86 in Fig. 3 of Adams).

Response to Arguments

9. Applicant's argument on pages 12-14 concerning that Mergard discloses neither a clock multiplier circuit nor how such a circuit would be connected within the microcontroller of Mergard. That argument is not persuasive because in Figs. 2-10 of Mergard clearly show that the clock multiplier circuit is inherently included within the microcontroller of Mergard. Note the above discussion with regard to claim 16. Therefore, the rejections to claims 1-3 and 8-15 of record are still believed to be proper and are therefore maintained as set forth above.

Allowable Subject Matter

10. Claims 4-7 and 12-13 are allowed.

The prior art of record fails to disclose or fairly suggest an microcontroller integrated circuit, as recited in claim 4, having specific structural limitations such as a frequency locked loop (340 in instant Fig. 4) further including a ramp generator (420), wherein the ramp generator starts a first ramp upon a first edge of the first signal (198), and wherein a first digital value indicative of a magnitude of the first ramp is determined upon a first edge of the second signal (196), and wherein the ramp generator starts a second ramp upon a second edge of the first signal, and wherein a second digital value indicative of a magnitude of the second ramp is determined upon a second edge of the second signal, the first and second digital values being used to generate a third digital value, the third digital value being supplied to the digital filter

(460), and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest an microcontroller integrated circuit, as recited in claim 12, having specific structural limitations such as the clock multiplier circuit (as shown in Fig. 9) includes a control loop (607, 609), the control loop including an oscillator (607) and a loop divider (639), the loop divider being a counter that is preset with a preset value (651), and wherein a phase of the second signal (618) is adjusted with respect to the first signal (REF CLOCK) by changing the preset value; such as the preset value a digital six, loop divider 639 therefore counts from the preset value of six, seven, eight. When the loop divider 639 transitions the count state eight, the feedback clock (641) transitions high (as illustrated in Figure 10). Loop divider 639 continues to count the count state rolls over from the terminal count sixteen to the count value Upon entering count state zero, the feedback clock FEEDBACK CLOCK transitions as illustrated in Figure 10. Because the synchronization pulse SYNC PULSE generated from the reference clock, changing the preset value to which the loop divider is preset can change the time 652 between the rising edge of the feedback clock and the falling edge of the reference clock; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
August 13, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800